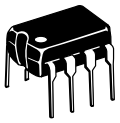
ASM1232LP, ASM1232LPS

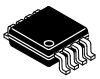
5 V μP Power Supply Monitor and Reset Circuit

ON Semiconductor®

http://onsemi.com

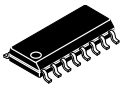


PDIP−8
P SUFFIX
CASE 646AA



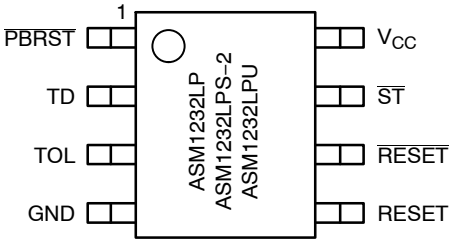
MICRO−8
U SUFFIX
CASE 846AA

SOIC−8
S SUFFIX
CASE 751BD

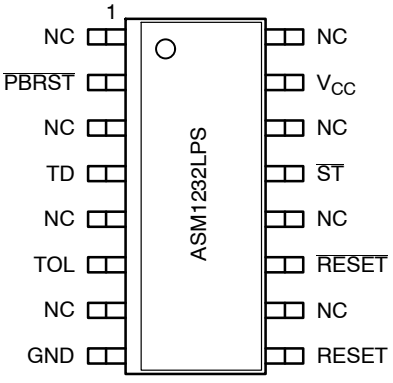


SOIC−16
S SUFFIX
CASE 751BG

PIN CONFIGURATIONS



DIP/SO/MicroSO
(Top View)



SO
(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

Description

The ASM1232LP/LPS is a fully integrated microprocessor Supervisor. It can halt and restart a “hung−up” microprocessor, restart a microprocessor after a power failure. It has a watchdog timer and external reset override.

A precision temperature−compensated reference and comparator circuits monitor the 5 V, V_{CC} input voltage status. During power−up or when the V_{CC} power supply falls outside selectable tolerance limits, both RESET and $\overline{\text{RESET}}$ become active. When V_{CC} rises above the threshold voltage, the reset signals remain active for an additional 250 ms minimum, allowing the power supply and system microprocessor to stabilize. The trip point tolerance signal, TOL, selects the trip level tolerance to be either 5% or 10%.

Each device has both a push−pull, active HIGH reset output and an open drain active LOW reset output. A debounced manual reset input, $\overline{\text{PBRST}}$, activates the reset outputs for a minimum period of 250 ms.

There is a watchdog timer to stop and restart a microprocessor that is “hung−up”. The watchdog timeouts periods are selectable: 150 ms, 610 ms and 1200 ms. If the $\overline{\text{ST}}$ input is not strobed LOW before the time−out period expires, a reset is generated.

Devices are available in 8−pin DIP, 16−pin SO and compact 8−pin MicroSO packages.

Features

- 5 V Supply Monitor
- Selectable Watchdog Period
- Debounce Manual Push−button Reset Input
- Precision Temperature−compensated Voltage Reference and Comparator
- Power−up, Power−down and Brown Out Detection
- 250 ms Minimum Reset Time
- Active LOW Open Drain Reset Output and Active HIGH Push−pull Output
- Selectable Trip Point Tolerance: 5% or 10%
- Low−cost Surface Mount Packages: 8−pin/16−pin SO, 8−pin DIP and 8−pin Micro SO Packages
- Wide Operating Temperature −40°C to +85°C (N Suffixed Devices)

Applications

- Microprocessor Systems
- Computers
- Controllers
- Portable Equipment
- Intelligent Instruments
- Automotive Systems

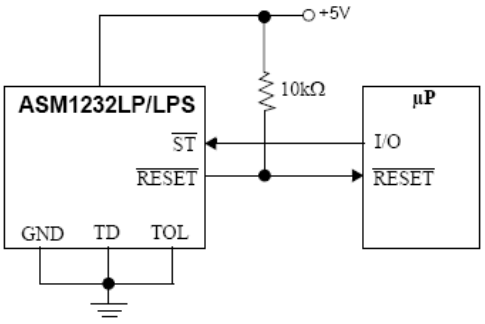


Figure 1. Typical Operating Circuit

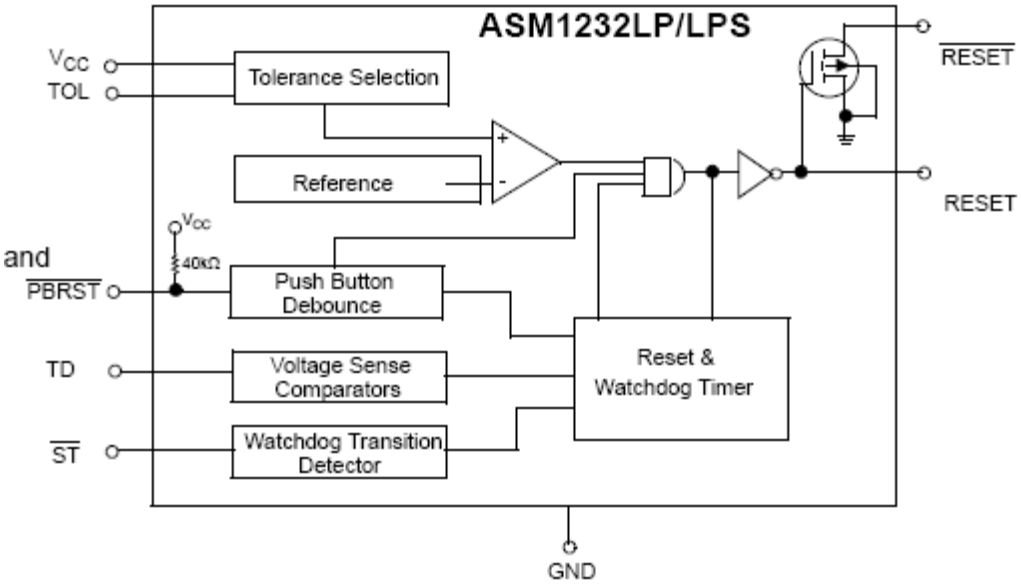


Figure 2. Block Diagram

Table 1. PIN DESCRIPTION

Pin # 8−Pin Package	Pin # 16−Pin Package	Pin Name	Function
1	2	$\overline{\text{PBRST}}$	Debounced manual pushbutton RESET input.
2	4	T_D	Watchdog time delay selection. (t_{TD} = 150 ms for T_D = GND, t_{TD} = 610 ms for T_D = Open, and t_{TD} = 1200 ms for T_D = V_{CC}).
3	6	T_{OL}	Selects 5% (T_{OL} connected to GND) or 10% (T_{OL} connected to V_{CC}) trip point tolerance.
4	8	GND	Ground.
5	9	RESET	Active HIGH reset output. RESET is active: 1. If V_{CC} falls below the reset voltage trip point. 2. If $\overline{\text{PBRST}}$ is LOW. 3. If $\overline{\text{ST}}$ is not strobed LOW before the timeout period set by T_D expires. 4. During power−up.
6	11	$\overline{\text{RESET}}$	Active LOW reset output. (See RESET).
7	13	$\overline{\text{ST}}$	Strobe input.
8	15	V_{CC}	5 V power.
	1,3,5,7,10,12,14,16	NC	No internal connection.

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter		Min	Max	Unit
Voltage on V_{CC} (Note 1)		−0.5	7	V
Voltage on $\overline{\text{ST}}$, TD (Note 1)		−0.5	V_{CC} + 0.5	V
Voltage on $\overline{\text{PBRST}}$, RESET, $\overline{\text{RESET}}$ (Note 1)		−0.5	V_{CC} + 0.5	V
Operating Temperature Range (N suffixed devices)		−40	+85	°C
Operating Temperature Range (others)		0	70	°C
Soldering Temperature (for 10 sec)			+260	°C
Storage Temperature		−55	+125	°C
ESD rating	HBM		2	KV
	MM		200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Voltages are measured with respect to ground

Table 3. DC ELECTRICAL CHARACTERISTICS (Unless otherwise stated, 4.5 V ≤ V_{CC} ≤ 5.5 V and over the operating temperature range of 0°C to 70°C (−40°C to +85°C. for N devices). All Voltages are referenced to ground.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		4.5		5.5	V
$\overline{ST}$ and $\overline{PBRST}$ Input High Level	V_{IH}		2		V_{CC} + 0.3	V
$\overline{ST}$ and $\overline{PBRST}$ Input Low Level	V_{IL}		−0.3		0.8	V
V_{CC} Trip Point (T_{OL} = GND)	V_{CCTP}		4.50	4.62	4.74	V
V_{CC} Trip Point (T_{OL} = V_{CC})	V_{CCTP}		4.25	4.37	4.49	V
Watchdog Timeout Period	t_{TD}	T_D = GND	62.5	150	250	ms
Watchdog Timeout Period	t_{TD}	T_D = V_{CC}	500	1200	2000	ms
Watchdog Timeout Period	t_{TD}	T_D Floating	250	610	1000	ms
Output Voltage	V_{OH}	I = −500 μA (Note 4)	V_{CC} − 0.5	V_{CC} − 0.1		V
Output Current	I_{OH}	Output = 2.4 V (Note 3)	−8	−10		mA
Output Current	I_{OL}	Output = 0.4 V	10			mA
Input Leakage	I_{IL}	(Note 2)	−1.0		1.0	μA
RESET Low Level	V_{OL}	(Note 4)			0.4	V
Internal Pull−up Resistor		(Note 2)		40		kΩ
Operating Current (CMOS)	I_{CC1}				30	μA
Input Capacitance	C_{IN}				5	pF
Output Capacitance	C_{OUT}				10	pF
$\overline{PBRST}$ Manual Reset Minimum Low Time	t_{PB}	$\overline{PBRST}$ = V_{IL}	20			ms
Reset Active Time	t_{RST}		250	610	1000	ms
$\overline{ST}$ Pulse Width	t_{ST}	(Note 5)	20			ns
V_{CC} Fail Detect to $\overline{RESET}$ or RESET	t_{RPD}			5	8	μs
V_{CC} Slew Rate	t_F	4.75 V to 4.25 V	300			μs
$\overline{PBRST}$ Stable LOW to RESET and $\overline{RESET}$ Active	t_{PDLY}				20	ms
V_{CC} Detect to RESET or $\overline{RESET}$ inactive	t_{RPU}	t_{RISE} = 5 μs	250	610	1000	ms
V_{CC} Slew Rate	t_R	4.25 V to 4.75 V	0			ns

2. $\overline{PBRST}$ is internally pulled HIGH to V_{CC} through a nominal 40 kΩ resistor.
3. $\overline{RESET}$ is an open drain output.
4. RESET remains within 0.5 V of V_{CC} on power−down until V_{CC} falls below 2 V. $\overline{RESET}$ remains within 0.5 V of ground on power−down until V_{CC} falls below 2.0 V.
5. Must not exceed the minimum watchdog time−out period (t_{TD}). The watchdog circuit cannot be disabled. To avoid a reset, $\overline{ST}$ must be strobed.

Detailed Description

The ASM1232LP/LPS monitors the microprocessor or micro controller power supply and generates reset signal, both active HIGH and Active LOW, that halt processor operation whenever the power supply voltage levels are outside a predetermined tolerance.

RESET and $\overline{\text{RESET}}$ outputs

RESET is an active HIGH signal developed by a CMOS push−pull output stage and is the logical opposite to $\overline{\text{RESET}}$.

$\overline{\text{RESET}}$ is an active LOW signal. It is developed with an open drain driver. A pull up resistor of typical value 10 kΩ to 50 kΩ is required to connect with the output.

Trip Point Tolerance Selection

The TOL input is used to determine the level V_{CC} can vary below 5 V without asserting a reset. With TOL connected to V_{CC}, RESET and $\overline{\text{RESET}}$ become active whenever V_{CC} falls below 4.5 V. RESET and $\overline{\text{RESET}}$ become active when the V_{CC} falls below 4.75 V if TOL is connected to ground.

After V_{CC} has risen above the trip point set by TOL, RESET and $\overline{\text{RESET}}$ remain active for a minimum time period of 250 ms. On power−down, once V_{CC} falls below the reset threshold $\overline{\text{RESET}}$ stays LOW and is guaranteed to be 0.4 V or less until V_{CC} drops below 1.2 V. The active HIGH reset signal is valid down to a V_{CC} level of 1.2 V also.

Tolerance Select	Tolerance	TRIP Point Voltage (V)		
		Min	Nom	Max
TOL = V_{CC}	10%	4.25	4.37	4.49
TOL = GND	5%	4.5	4.62	4.74

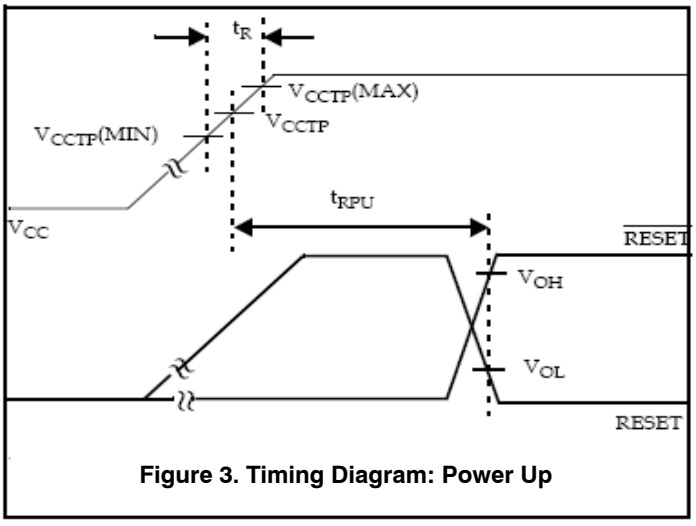


Figure 3. Timing Diagram: Power Up

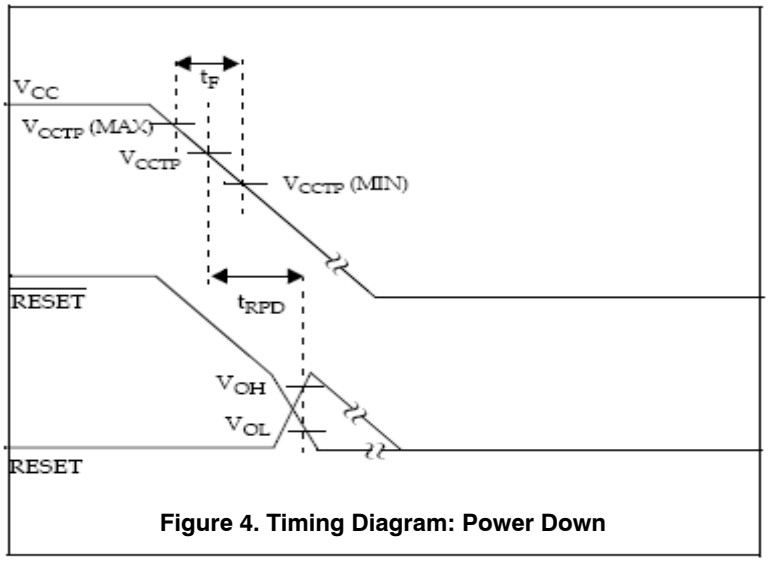


Figure 4. Timing Diagram: Power Down

Application Information

Manual Reset Operation

Push−button switch input, $\overline{\text{PBRST}}$, allows the user to override the internal trip point detection circuits and issue reset signals. The pushbutton input is debounced and is pulled HIGH through an internal 40 kΩ resistor.

When $\overline{\text{PBRST}}$ is held LOW for the minimum time t_{PB}, both resets become active and remain active for a minimum time period of 250 ms after PBRST returns $\overline{\text{HIGH}}$.

The debounced input is guaranteed to recognize pulses greater than 20 ms. No external pull−up resistor is required, since $\overline{\text{PBRST}}$ is pulled HIGH by an internal 40 kΩ resistor.

The $\overline{\text{PBRST}}$ can be driven from a TTL or CMOS logic line or shorted to ground with a mechanical switch.

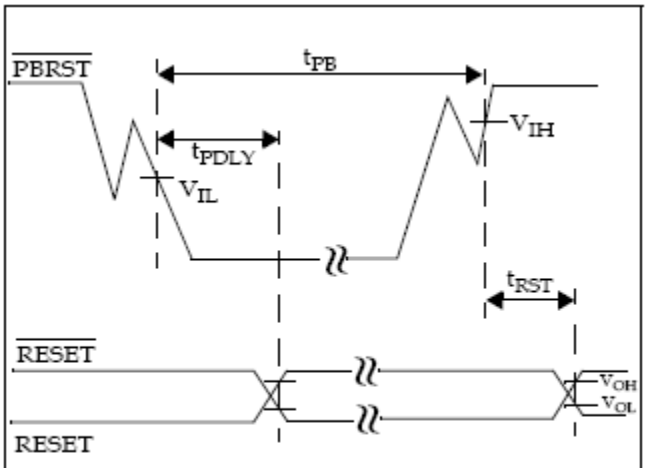


Figure 5. Timing Diagram: Pushbutton Reset

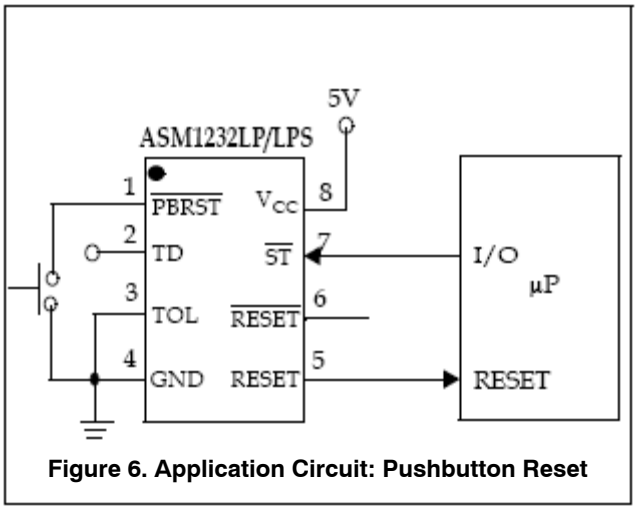


Figure 6. Application Circuit: Pushbutton Reset

Watchdog Timer and $\overline{ST}$ Input

A watchdog timer stops and restarts a microprocessor that is "hung−up". The μP must toggle the $\overline{ST}$ input within a set period (as selectable through TD input) to verify proper software execution. If the $\overline{ST}$ is not toggled low within the minimum timeout period, reset signals become active. In power−up after the supply voltage returns to an in−tolerance condition, the reset signal remains active for 250 ms minimum, allowing the power supply and system microprocessor to stabilize. $\overline{ST}$ pulses as short as 20 ns can be detected.

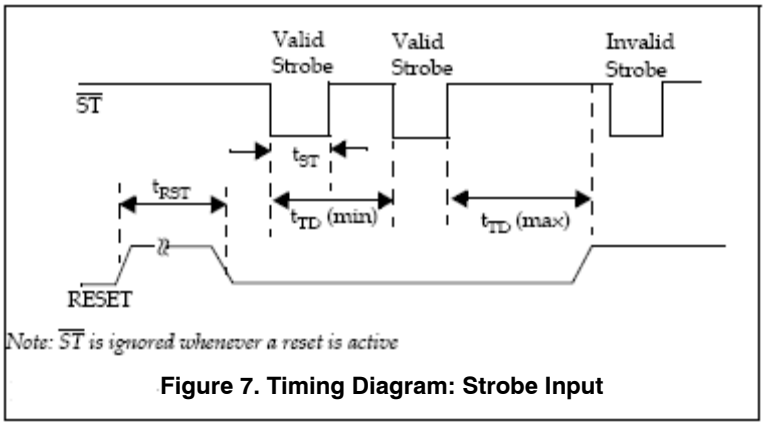


Figure 7. Timing Diagram: Strobe Input

Timeouts periods of approximately 150 ms, 610 ms or 1,200 ms are selected through the TD pin.

TD Voltage level	Watchdog Time−out Period (ms)		
	Min	Nom	Max
GND	62.5	150	250
Floating	250	610	1000
V_{CC}	500	1200	2000

The watchdog timer cannot be disabled. It must be strobed with a high−to−low transition to avoid watchdog timeout and reset.

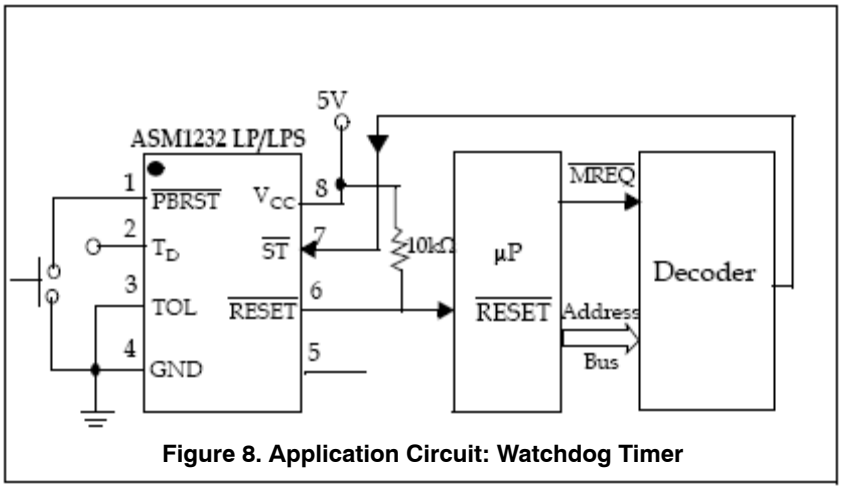
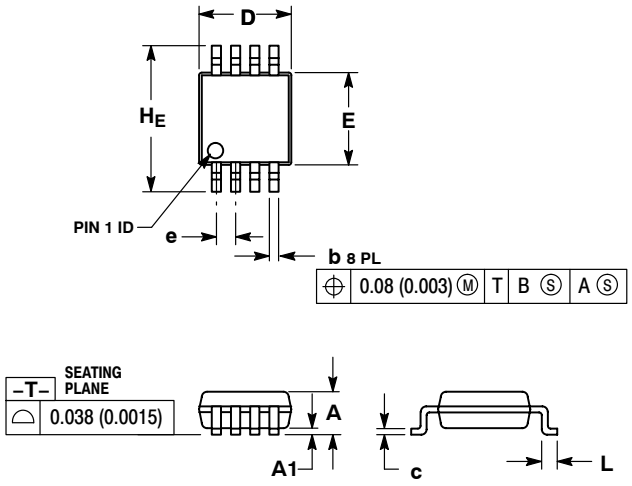


Figure 8. Application Circuit: Watchdog Timer

PACKAGE DIMENSIONS

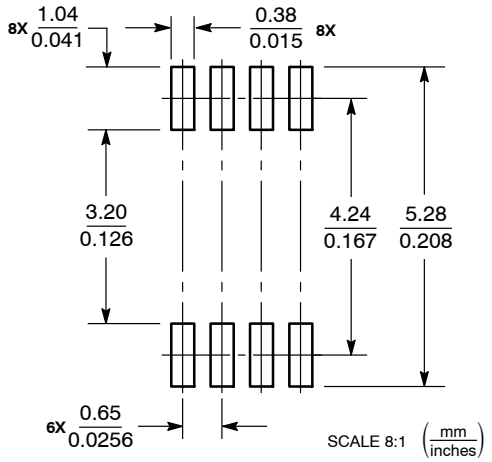
Micro8™ /TSSOP8 3x3
CASE 846AA−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A−01 OBSOLETE, NEW STANDARD 846A−02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	−−	−−	1.10	−−	−−	0.043
A1	0.05	0.08	0.15	0.002	0.003	0.006
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
e	0.65 BSC			0.026 BSC		
L	0.40	0.55	0.70	0.016	0.021	0.028
H_E	4.75	4.90	5.05	0.187	0.193	0.199

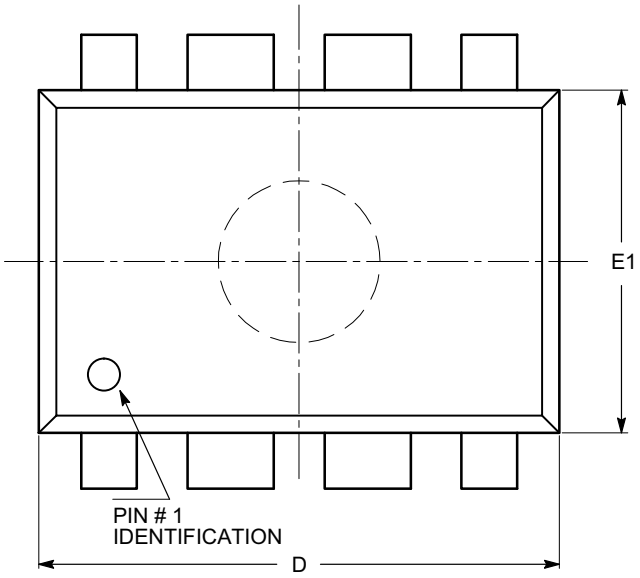
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

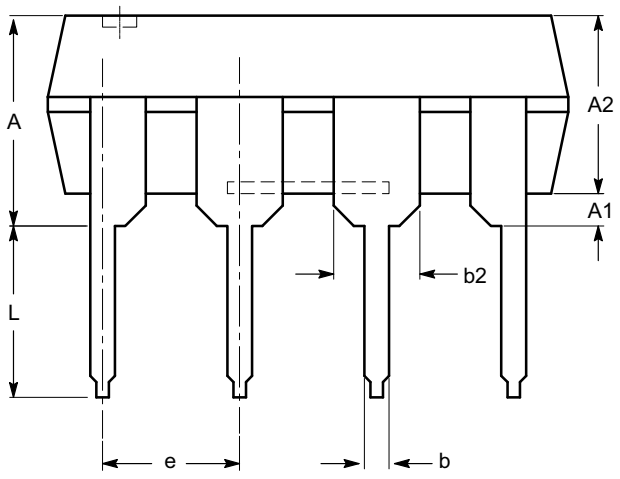
PACKAGE DIMENSIONS

PDIP−8, 300 mils
CASE 646AA−01
ISSUE A

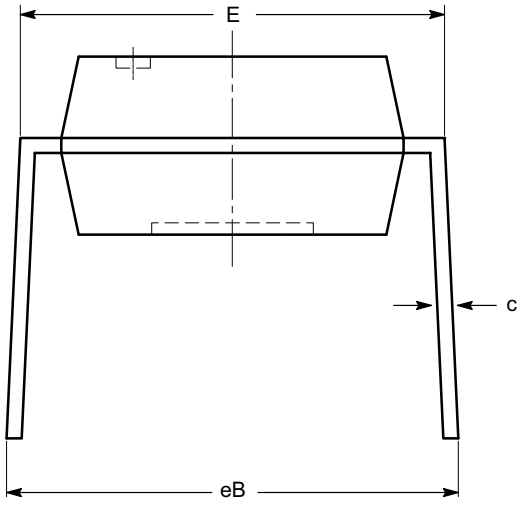


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.25
E1	6.10	6.35	7.11
e		2.54 BSC	
eB	7.87		10.92
L	2.92	3.30	3.80



SIDE VIEW

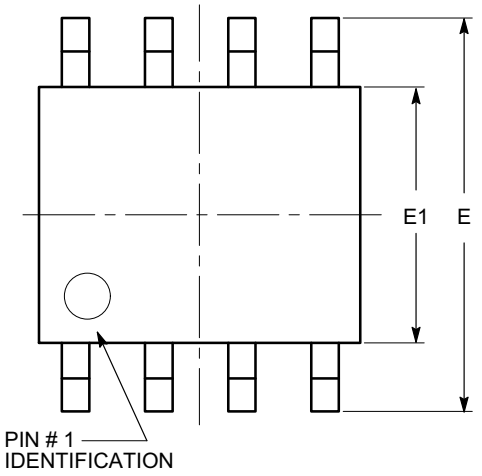


END VIEW

Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MS-001.

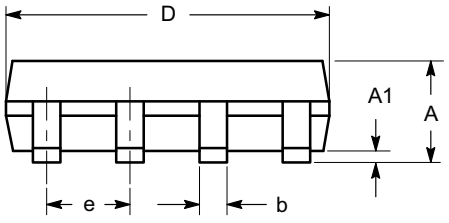
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

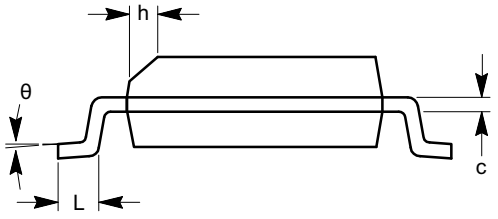


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW

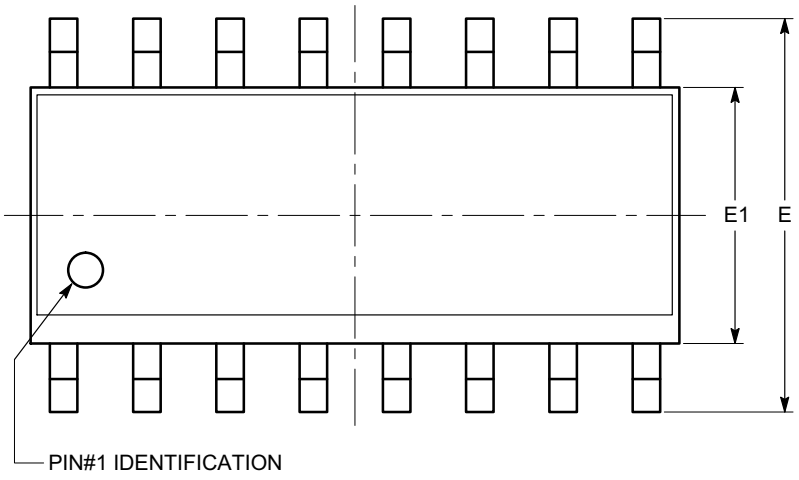


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

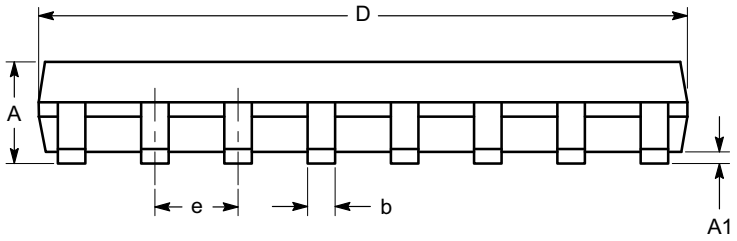
PACKAGE DIMENSIONS

SOIC−16, 150 mils
CASE 751BG−01
ISSUE O

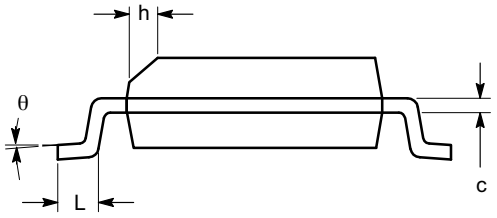


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0°		8°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

Table 4. ORDERING INFORMATION

Part Number (Note 6)	**Package**	**Operating Temperature Range**	**Maximum Supply Current (μA)**	**Voltage Monitoring Application**	**Package Marking**
TIN−LEAD DEVICES					
ASM1232LP	8L PDIP	0°C to +70°C	30	5 V	ASM1232LP
ASM1232LPN	8L PDIP	−40°C to +85°C	30	5 V	ASM1232LPN
ASM1232LPS	16L SOIC	0°C to +70°C	30	5 V	ASM1232LPS
ASM1232LPS−2	8L SOIC	0°C to +70°C	30	5 V	ASM1232LPS−2
ASM1232LPSN	16L SOIC	−40°C to +85°C	30	5 V	ASM1232LPSN
ASM1232LPSN−2	8L SOIC	−40°C to +85°C	30	5 V	ASM1232LPSN−2
ASM1232LPU	8L MSOP	0°C to +70°C	30	5 V	ASM1232LP
ASM1232LPUN	8L MSOP	−40°C to +85°C	30	5 V	ASM1232LPN
LEAD FREE DEVICES					
ASM1232LPF	8L PDIP	0°C to +70°C	30	5 V	ASM1232LPF
ASM1232LPNF	8L PDIP	−40°C to +85°C	30	5 V	ASM1232LPNF
ASM1232LPS−2F	8L SOIC	0°C to +70°C	30	5 V	ASM1232LPS−2F
ASM1232LPSF	16L SOIC	0°C to +70°C	30	5 V	ASM1232LPSF
ASM1232LPSN−2F	8L SOIC	−40°C to +85°C	30	5 V	ASM1232LPSN−2F
ASM1232LPSNF	16L SOIC	−40°C to +85°C	30	5 V	ASM1232LPSNF
ASM1232LPUF	8L MSOP	0°C to +70°C	30	5 V	ASM1232LPF
ASM1232LPUNF	8L MSOP	−40°C to +85°C	30	5 V	ASM1232LPNF

6. For parts to be packed in Tape and Reel, add "−T" at the end of the part number.

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